**SURNAME, NAME: GROUP:**

**Problem 1 (2.5 points; 25 minutes)**

1. Obtain the representation of A=111010102 in the following number systems (0,5p):

|  |  |
| --- | --- |
| Decimal |  |
| Octal |  |
| Hexadecimal |  |

1. Given the number B = 011111101CA2 represented in 2's-complement, obtain the decimal representation (0,5p).
2. Perform the following operations using 2's complement representations: X=A+B e Y=-B-A. Explain if there is overflow in the operation (1,5p).

**SURNAME, NAME: GROUP:**

**Problem 2 (4 points; 40 minutes)**

Given the following VHDL code:

ENTITY Combinacional IS

PORT (

A,C:   IN  STD\_LOGIC;

B:     IN STD\_LOGIC\_VECTOR  ( 1 downto 0) ;

F1,cout: OUT STD\_LOGIC;

F2: OUT  STD\_LOGIC\_VECTOR (1 downto 0) );

END Combinacional;

ARCHITECTURE funcional OF Combinacional IS

Signal X,Z: STD\_LOGIC;

Signal Y: STD\_LOGIC\_VECTOR (3 downto 0);

Signal AUX:UNSIGNED (2 downto 0);

BEGIN

X<= A XOR B(1);

 PROCESS (\_  \_ \_ \_ \_ \_ \_ \_ \_ \_ \_ \_ \_ \_ \_ )

    BEGIN

        IF X='1' THEN

            IF B(0)='0' THEN

            F1<= C;

            ELSE F1<= NOT (A);

            END IF;

        Z<= NOT (A);

        ELSE F1<=A OR B(1) OR C; Z<=C AND B(1);

        END IF;

    END PROCESS;

    Y<= "0011" WHEN B="00" ELSE

            "0101" WHEN B="01" ELSE

            "1101" WHEN B="10" ELSE

            "1111" WHEN B="11" ELSE

            "1101";

AUX<= resize (UNSIGNED (Y(1 downto 0)),3)+ resize (UNSIGNED(Y(3 downto 2)),3);

cout <= AUX(2);

F2<=std\_logic\_vector(AUX(1 downto 0));

END funcional;

1. (5%) Indicate all the inputs and outputs of the circuit and their number of bits.
2. (5%) Fill the sensitivity list of the process
3. (30%) Obtain the truth table for X and Z.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **C** | **A** | **B(1)** | **X** | **Z** |
|  |  |  |  |  |
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1. (30%) Fill the chronogram for F1

Gráfico, Tabla

Descripción generada automáticamente

1. (30%) According to the chronogram, obtain the value of F2 and Cout at the following times. Justify your answer
   * t=7 ns
   * t=27 ns
   * t=42 ns

**Problem 3 (3.5 points; 35 minutes)**

The control circuit of an industrial machine has 4 sensors (A,B,C and D) and 3 alarm lights (X, Y, Z). The specification of the circuit is as follows:

* If signal A is not active, all lights will go off.
* If enable signal A is active:
* Alarm light X will turn on when sensors B and C are the same but different from D.
* Alarm light Y will turn on when 2 consecutive sensors are on in the order of B, C and D.
* Alarm light Z will turn on when sensors B and D have different value.

All signals are active by high level.

1. Write the truth table of the circuit following the order of inputs and outputs described in the statement. Write the first abbreviated canonical form of the functions X, Y and Z (0.5 p.).
2. Implement function Y with a decoder with 3 data inputs and an enable input, and the necessary logic gates (0.75 p.).
3. Implement the Z function with a 3-input select multiplexer (0.75 p.)
4. Describe the system **architecture** in VHDL assuming that the sensors and lights have been properly defined in the entity. (1,5p)